Notice of Allowability	Application No.	Applicant(s)	
	10/690,417	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 12 October 2005*.

2. ☒ The allowed claim(s) is/are *1-13,15-17,19-37,39 and 46-59*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

This office action is in response to the filing of the amendment on 12 October 2005. Claims 1-13, 15-17, 19-37, 39 and 46-59 are pending; claims 14, 18, 38 and 40-45 have been cancelled.

Allowable Subject Matter

Claims 1-13, 15-17, 19-37, 39 and 46-59 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest referring to claim 1, prior art does not disclose teach or suggest etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer; and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Referring to claims 21, prior art does not disclose teach or suggest etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel; forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel; and separating the

semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages.

Referring to claim 38, prior art does not disclose teach or suggest etching the passive surface of the semiconductor wafer concurrently with etching the plurality of semiconductor die side surfaces.

For example, Takahashi et al. (5,977,641) disclose a method of forming chip-scale packages including providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; cutting at least one channel in the active surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die surfaces; forming a protective coating on the semiconductor wafer to cover the active surface and fill the at least one channel; and separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages.

However, Takahashi et al. do not disclose, anticipate, teach, or suggest etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel; etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer, wherein etching the passive surface of the semiconductor wafer is done concurrently with etching the plurality of semiconductor die side surfaces; forming a

second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Shelton et al. (6,849,524) disclose a method of forming chip-scale packages including providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; forming a protective coating on the semiconductor to cover the active surface (step 410); cutting at least one channel in the active surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die surfaces (Step 440); etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects (Step 550); and separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages (Step 560).

However, Shelton et al. do not disclose, anticipate, teach or suggest etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer, wherein etching the passive surface of the semiconductor wafer is done concurrently with etching the plurality of semiconductor die side surfaces; forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

The prior art made of record in this action does not anticipate, teach, or suggest etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel; etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer, wherein etching the passive surface of the semiconductor wafer is done concurrently with etching the plurality of semiconductor die side surfaces; forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Supervisory ZANDRA V. SMITH
PRIMARY EXAMINER
11/22/05